

**United States Patent Application for:**

**ANODIC BONDING OF A STACK OF CONDUCTIVE  
AND GLASS LAYERS**

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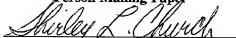
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## ANODIC BONDING OF A STACK OF CONDUCTIVE AND GLASS LAYERS

### Field of the Invention:

The present invention relates to a method of bonding alternating conductive and glass layers. More particularly, the method pertains to anodic bonding of stacks of alternating conductive and glass layers, where the conductive layer is a metal or semiconductor. The invention has applicability, among other areas, in the formation of such stacks for microcolumns in electron optics, including electron microscopes and lithography apparatus, in the formation of micro electromechanical structures (MEMS), and also in micro opto-electromechanical structures (MOEMS).

### Background of the Invention:

Stacks of alternating layers of conductive material and glass find use in a number of practical applications such as in electron optics and micro electromechanical structures. Anodic bonding has been one of the techniques used to bond the conductive layer to the glass layer. In some instances, a semiconductor material such as silicon is used as the conductive layer, and the glass layer is a borosilicate glass, such as PYREX® (Corning Glass, Corning, New York) or BOROFLOAT® (Schott Glass Technologies, New York, New York). In the alternative, the glass layer may be a lithium aluminosilicate -  $\beta$ -quartz glass-ceramic such as Prototype PS-100 available from HOYA Co., Tokyo, Japan. The advantage of this latter glass is that anodic bonding may be performed at a temperature below about 180 °C.

A detailed description of use of the HOYA Co. Lithium aluminosilicate -  $\beta$ -quartz glass-ceramic glass is provided in a publication by Shuichi Shoji et al. entitled: "Anodic Bonding Below 180 °C For Packaging And Assembling Of MEMS Using Aluminosilicate- $\beta$ -quartz Glass-Ceramic", available from IEEE as document 0-7803-

1 3744-1/97, the subject matter of which is hereby incorporated by reference in its entirety.  
2 In particular the bonding of Prototype PS-100 glass-ceramic pieces 370  $\mu\text{m}$  thick to  
3 silicon wafers was achieved using anodic bonding at a temperature ranging from about  
4 140 °C to about 180 °C, at an applied DC voltage ranging from about 300 V to about  
5 700 V, over a time period of about 10 minutes or less. A comparison is made for bonding  
6 the Prototype PS-100 glass relative to #7740 Corning PYREX® glass and relative to  
7 #SD-2 HOYA Bonding Glass. In all cases, a single layer of glass is bonded to a layer of  
8 silicon.

9 One conventional approach to anodic bonding is shown in Figure 1. In this  
10 Figure, conductive layers (silicon layers, by way of example) 108, 110, 112, and 114 are  
11 alternated with electrically insulating layers (borosilicate glass, by way of example) 107,  
12 109, and 111. The stack 100 of alternating silicon and glass layers is placed upon a  
13 hotplate 106, which provides both a source of heat input and electrical grounding.  
14 Electrical contact 102 is contacted to uppermost silicon layer 108, while electrical contact  
15 104 is contacted to the hotplate 106. Silicon layer 108 acts as the upper electrode, while  
16 silicon layer 114/ hotplate 106 acts as the lower electrode. Heat is applied to the hotplate  
17 106 and a voltage is applied between the electrodes 108 and 114/106, through all of the  
18 layers to be bonded. The heated glass acts as an electrochemical cell and permits the  
19 transfer of current through the borosilicate glass layers 107, 109, and 111. The  
20 application of the voltage causes ionized sodium and oxygen to move within the glass and  
21 promotes bonding of silicon layer surfaces to glass layer surfaces.

22 Looking at the process in a little more detail, anodic bonding has been  
23 accomplished using either DC voltage or AC voltage. Accordingly, for purposes of the  
24 following description, the voltage source in Figure 1 is shown in conceptual, rather than  
25 structural form.

1 In the DC voltage technique, a negative DC potential is applied between electrodes  
2 108 and 114/106, followed by application of reverse polarity DC potential between the  
3 electrodes 108 and 114/106.

4 When, for example, electrode 114/106 is at ground potential, and electrode 108 is  
5 at a negative potential, oxygen ions travel toward surface 132 of glass layer 107; surface  
6 134 of glass layer 109; and, surface 136 of glass layer 111. This enables the covalent  
7 bonding of oxygen to silicon at surface 132 between glass layer 107 and silicon layer 110;  
8 at surface 134, between glass layer 109 and silicon layer 112; and, at surface 136, between  
9 glass layer 111 and silicon layer 114. Simultaneously, application of the DC voltage in  
10 this manner causes sodium ions that are part of the glass layers to move toward the  
11 opposite surface of each glass electrochemical cell. For example, sodium ions move  
12 toward surface 131 of glass layer 107; surface 133 of glass layer 109; and, surface 135 of  
13 glass layer 111.

14 The series connection of the electrochemical cells creates a potential gradient over  
15 the entire stack. Since current flows throughout the stack 100, from top electrode 108 to  
16 bottom electrode 114/106, each silicon layer acting as an electrode, the electrode surface  
17 includes the entire major surface of each of the stacked silicon layers.

18 After application of the DC potential in this fashion, in the next step in the anodic  
19 bonding process, the voltage is reversed, such that electrode 114/106 is at a negative  
20 potential, and electrode 108 is at ground. This permits oxygen ions to move within glass  
21 layer 107 toward surface 131; within glass layer 109 toward surface 133; and within glass  
22 layer 111 toward surface 135. However, the covalent bonding of the oxygen to the silicon  
23 at surfaces 131, 133, and 135 is weaker due to the presence of the sodium compounds  
24 120, 122, and 124, respectively, which form due to the movement of sodium ions toward  
25 these surfaces during the bonding process. Simultaneously with the covalent bonding of  
26 surfaces 131, 133, and 135, sodium compounds 126, 128, and 130 form at surfaces 132,

1 134, and 136 of glass layers 107, 109, and 111, respectively, weakening the bond between  
2 these glass surfaces and the mating silicon surfaces.

3 In view of the weakened bonds formed at silicon surfaces 131, 133 and  
4 135, as described above, an AC voltage anodic bonding technique was devised. By  
5 applying an AC voltage, voltage polarities are reversed continuously, thus achieving  
6 bonding between all adjoining surfaces of consecutive layers. By applying AC voltage,  
7 the concentration of sodium at each interface during bonding is gradually increased during  
8 the bonding period. This means the amount of sodium contamination is lower at the  
9 beginning of the bonding process, which better facilitates bonding. However, by the end  
10 of the process the sodium contamination has reached a significant level, and the overall  
11 bond strength between the alternating layers may not be adequate for some applications.

12 In view of the foregoing deficiencies, it would be desirable to be able to bond  
13 semiconductor and glass layers anodically, without the concentration of sodium and  
14 sodium compounds at the interface of bonding layers.

### 15 SUMMARY OF THE INVENTION

16 We have developed a method of anodic bonding which directs cations to a  
17 location within a bonding structure which is away from critical bonding surfaces. This  
18 prevents the formation of compounds comprising the cations at the critical bonding  
19 surfaces. The anodic bonding electrode contacts are made in a manner which  
20 concentrates the cations and compounds thereof in a portion of the bonded structure  
21 which can be removed, or cleaned to remove the compounds from the structure. A device  
22 formed from the bonded structure contains minimal, if any, of the cation-comprising  
23 compounds which weaken bond strength within the structure. In the alternative, the  
24 cations and compounds thereof are directed to a portion of the bonding structure which  
25 does not affect the function of a device which includes the bonded structure.

**BRIEF DESCRIPTION OF THE DRAWINGS**

The foregoing and other aspects of the invention will be appreciated from the following detailed discussion, provided in conjunction with the accompanying drawings, in which:

Figure 1 shows a schematic of a cross-section of layers bonded using a conventional anodic bonding approach.

Figure 2 shows a schematic of a cross-section of layers bonded in accordance with one embodiment of the invention.

Figure 3A shows a schematic of a cross-section of a stack of layers bonded in accordance with a second embodiment of the invention.

Figure 3B shows a schematic of an enlarged top view of a portion of the upper surface of the stack of layers shown in Figure 3A.

Figures 4A and 4B show a schematic of a cross-section of a starting stack of pre-bonded layers and the same stack after a third layer has been bonded (using a conventional anodic bonding method), respectively.

Figure 4C shows an enlargement of a bonded area of Figure 4B, for purposes of showing an area in which sodium accumulates during bonding, leading to the formation of undesirable sodium compounds.

1           Figures 5A and 5B show a schematic of a cross-section of a starting stack of pre-  
2 bonded layers and the same stack after a third layer has been bonded (using a technique  
3 in accordance with the invention), respectively.

4           Figure 5C shows an enlargement of a bonded area of Figure 5B, for purposes of  
5 showing the absence of sodium accumulations during bonding, for purposes of  
6 comparison with Figure 4C.

7           Figure 6 shows a schematic of a cross section of layers bonded using the method  
8 of the invention where extended electrodes which contact respective types of layers are  
9 employed.

#### 10                           **DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS**

11           As a preface to the detailed description, it should be noted that, as used in this  
12 specification and the appended claims, the singular forms of "a", "an", and "the" include  
13 plural referents, unless the context clearly dictates otherwise. Thus, for example, the term  
14 "a semiconductor" includes a variety of different materials which are known to have the  
15 behavioral characteristics of a semiconductor; reference to "a metal" includes, for  
16 example, aluminum, aluminum alloys, copper, copper alloys, tungsten, tungsten alloys,  
17 iridium, iridium alloys, platinum, platinum alloys, and other conductive materials which  
18 would be suitable in the application described.

19           We have discovered that during the anodic bonding of a glass layer to a  
20 conductive layer, undesirable sodium compounds form on a glass surface which is in  
21 contact with a surface acting as a negative electrode. The extent of this compound  
22 formation is so pervasive as to cause major bonding problems, and to even prevent  
23

1 bonding in some instances. With reference to Figure 1, once again, the sodium ions  
2 which have moved to glass layer surfaces during an anodic bonding process react with  
3 ambient materials found at the glass surface, forming sodium compounds such as sodium  
4 hydroxide or sodium carbonate. These compounds are shown in Figure 1 as black boxes  
5 120 on glass surface 131; black boxes 126 on glass surface 132; black boxes 122 on glass  
6 surface 133; black boxes 128 on glass surface 134; black boxes 124 on glass surface 135;  
7 and, black boxes 130 on glass surface 136. Because sodium is so reactive, such  
8 compounds form readily.

9 As previously described, in the bonding process where DC potential is applied,  
10 bonding is achieved in two steps. In the first step, for example, with silicon layer 108  
11 acting as a negative electrode, bonding is achieved at glass surfaces 132, 134, and 136;  
12 and then, in a second step, the potential is reversed to achieve bonding at glass surfaces  
13 131, 133, and 135. During the first step, sodium compounds 120, 122, and 124 form over  
14 the entire major surfaces 131, 133, and 135 of the borosilicate glass layers 107, 109, and  
15 111, respectively. During the second bonding step, because of the presence of these  
16 sodium compounds on the glass surfaces 131, 133, and 135, bonds which are formed are  
17 very weak. For microcolumn applications, for example, those bonds may be so weak as  
18 to be ineffectual. In addition, the formation of sodium compounds on the entire major  
19 surfaces 132, 134, and 136 of glass layers 107, 109, and 111 during the second bonding  
20 step weakens the bonds previously formed at these glass surfaces.

21 The strength of the bond achieved may be adequate for some applications, but the  
22 presence of sodium compounds formed at the various bonding surfaces and at adjacent  
23 surfaces to which sodium migrates (due to concentration gradients) may cause severe  
24 device performance problems. For example, when sodium reacts with water in the air, it  
25 forms sodium hydroxide, a highly corrosive compound which can react with silicon and  
26 other materials and cause damage. In some electro-optical applications, where there is a  
27 thin silicon membrane at a glass interface, the sodium hydroxide may etch completely



1 through the membrane. In electronic circuits, sodium may react with doped silicon in a  
2 transistor device, eventually causing a short in the device.

3 Due to our discovery of how extensive and pervasive the sodium compounds  
4 were, it was critical to develop a method of anodic bonding in which the undesirable  
5 sodium compounds are directed toward an area of the bonding structure which is away  
6 from critical bonding surfaces. Preferably, the sodium compounds are concentrated at a  
7 location within the bonding structure which can be removed from the bonded structure, or  
8 where the compounds can be cleaned from the glass surface.

9 The method of the invention is, in fact, generally applicable to the bonding of any  
10 two layers where an electrochemical cell can be formed between the two layers; and,  
11 although the invention is described with respect to the bonding of a glass to a conductive  
12 layer, one skilled in the art, after reading this disclosure, will understand that another,  
13 second material (other than a glass as it is commonly defined) may be substituted for the  
14 glass, so long as the second material is capable of performing the function necessary to  
15 permit anodic bonding. The second material should provide the effective formation of an  
16 electrochemical cell during the bonding process. Glass has been known to be well-suited  
17 for this purpose, because it contains charge transfer ions which facilitate the formation of  
18 electrochemical cells and enable the anodic bonding process. However; it is within the  
19 contemplation of the invention that other suitable materials capable of enabling the  
20 formation of electrochemical cells, including materials which may be devised in the  
21 future, may be used.

22 In addition to constraints related to the formation of an electrochemical cell, there  
23 are thermal constraints, *i.e.* the second material should have thermal expansion  
24 characteristics that compare favorably to those of the conductive material to which the  
25 second material is bonded.

26 Electrodes used in the anodic bonding process are contacted with layers to be  
27 bonded in a manner such that cations and compounds thereof are concentrated in a portion

1 of the bonded structure which can be removed, or cleaned to remove the compounds from  
2 the structure. In the alternative, the cations and compounds thereof are directed to a  
3 portion of the bonded structure which does not affect the function of a device which  
4 includes the bonding structure.

5 For example, in applications where a wafer-sized structure is bonded and chips are  
6 later diced out of the wafer, the electrode contact areas can be removed during the dicing  
7 operation. In applications where a chip-sized structure is bonded, the electrode contact  
8 areas can be designed to be accessible to a water rinse for removal of sodium compounds.  
9 In the alternative, depending on the device and the probability for subsequent harm to  
10 device performance, the electrode contact areas may be placed at the edge of a chip stack.

11 In one particularly useful embodiment of the invention, alternating semiconductor  
12 (or metal) and glass layers in a stack are anodic bonded by contacting electrodes to  
13 consecutive layers in the stack, rather than contacting electrodes only to the top and  
14 bottom layers of the stack. With this technique, there are two effects. First, the glass  
15 electrochemical cells are in parallel, rather than in series. A second, attendant effect is  
16 that there is no longer a potential gradient throughout the stack. Instead, the only potential  
17 gradient is between consecutive layers.

18 Because of these effects, sodium compounds, which form from sodium ions  
19 generated within the glass during the anodic bonding process, only form in the vicinity of  
20 the electrodes, rather than across the entire major surfaces of the layers. In particular, the  
21 semiconductor or metal layers no longer act as electrodes themselves. As a result, the  
22 bonding between the semiconductor (or metal) and glass layers is relatively unaffected by  
23 the presence of sodium compounds.

24 In one variation of the embodiment, each layer is contacted separately, with  
25 separate electrode contacts. In another variation, larger, extended electrodes are used to

1 contact respective types of layers. The electrodes may contact a limited area on a major  
2 surface or may contact a minor surface of the associated layers.

3 Referring now to Figure 2, which illustrates one embodiment of the invention,  
4 electrodes 203, 205, 207, and 209 contact respective silicon layers 108, 110, 112, and  
5 114; while electrodes 202, 204, and 206 contact respective glass layers 107, 109, and 111.  
6 While the electrodes are shown conceptually as contacting a minor surface of the layers,  
7 in fact, as will be explained below, the electrodes may contact either a limited portion of a  
8 major surface or a minor surface of the layers. The shape of the electrodes is not  
9 significant for purposes of explaining the principles underlying the invention, and so the  
10 electrodes are shown in schematic, rather than structural form.

11 With respect to Figure 2, when a negative potential is applied between the silicon  
12 layers and the glass layers, the following electrochemical cells are formed: a first cell  
13 comprises layers 108, 107, and 110; a second cell comprises layers 110, 109, and 112; and  
14 a third cell comprises layers 112, 111, and 114. With the depicted arrangement, because a  
15 separate electrodes contact each of the layers, the electrochemical cells are formed in  
16 parallel, rather than in series. With this parallel configuration, all of the bonding of the  
17 layers occurs in a single step of applying a negative potential. In each of these cells, of  
18 course, there is an electrical potential, but there is no potential gradient across the entire  
19 stack, because the resulting electrochemical cells are formed in parallel, rather than in  
20 series. The formation of electrochemical cells in this manner prevents the major surfaces  
21 of silicon layers 108, 110, 112, and 114 from acting as negative electrodes where sodium  
22 compounds are formed. Consequently, sodium compounds will not form across the  
23 interfaces between the silicon and glass layers. The compounds may form where the  
24 electrodes contact these various layers, but bonding between the layers (which occurs at

1 the major surfaces of the layers) will not be affected by the sodium compounds formed at  
2 the electrode contact points.

3 In accordance with the method of the invention, when the glass layer being bonded  
4 is PYREX ®, the hotplate 106 is heated, for example, to a temperature between about  
5 300° C and about 500° C (other temperatures also may be suitable, depending on the  
6 particular glass used). A DC voltage of, for example, from -0.2 kV to -2.0 kV, is  
7 provided to the glass layers, with the silicon layers being grounded. Excellent results  
8 have been obtained for voltages within the range of -0.3 kV to -1.0 kV. The foregoing  
9 voltage is exemplary; what matters more is that there is a negative potential difference  
10 between the silicon layers and the glass layers, *i.e.*, the silicon layers should be at a higher  
11 potential than the glass layers. In one experiment, in which five silicon layers and four  
12 interleaved glass layers were bonded in a single 6 mm x 6 mm chip stack, a satisfactory  
13 bonding of the layers was achieved using -0.5 kV at about 450 °C for a time period of  
14 about 5 minutes. In another experiment, where five silicon layers and four interleaved  
15 glass layers were bonded in a single 4 inch diameter wafer stack, a satisfactory bonding of  
16 the layers was achieved using -1.0 kV at about 400 °C for a time period of about 30  
17 minutes. Factors which must be considered in determining the amount of time which  
18 will be required for bonding include, but are not limited to, the applied voltage, the  
19 temperature of the substrate, the surface area of the contact electrode, the glass surface  
20 area to be bonded in combination with the geometry of the glass electrical contact surface  
21 area, and the distance ions must travel to promote the bonding.

22 It is important to mention that the applied voltage is independent of the number of  
23 layers in the stack. In fact, the number of layers in the stack may vary as desired. For the  
24 sake of achieving the goal of avoiding formation of sodium compounds, bonding should  
25 be effected among at least two layers of a first material, and an interleaved layer of a

1 second material. There could be two layers of semiconductor or metal, and an interleaved  
2 layer of glass; or there could be two layers of glass, and an interleaved layer of  
3 semiconductor or metal. The application of an appropriate potential is based on the  
4 sequencing of the layers.

5 The inventive technique contrasts with the technique previously described with  
6 reference to Figure 1. For example, a relatively higher voltage, for example, -2 kV was  
7 applied on the upper silicon layer 108 of stack 100 for a time period of about 5 minutes at  
8 a stack temperature of about 450 °C, followed by reversal of the potential to +2 kV for a  
9 period of about 15 minutes. During application of the -2kV to silicon layer 108, glass  
10 surfaces 131, 133 and 135 were bonded to the silicon layer surfaces with which they were  
11 in contact. However, simultaneously, undesirable silicon compounds were formed on  
12 glass surfaces 132, 134, and 136. Upon reversal of the voltage to +2kV, sodium  
13 compounds were formed on the already bonded interfaces including glass surfaces 131,  
14 133, and 135. In addition, due to the presence of undesirable silicon compounds on glass  
15 surfaces 132, 134, and 136, only a weak bond was formed between these glass surfaces  
16 and the silicon layer surfaces with which they were in contact. The longer the period of  
17 time required for the first bonding process, the higher the probability that a good bond  
18 will not be obtained in the second bonding process. We observed that even longer  
19 bonding times, higher bonding temperatures and the use of higher voltages did not  
20 provide acceptable bonding during the second bonding process in many instances.

21 As previously mentioned, use of an alternating current rather than a reversing DC  
22 current may reduce the probability of bonding failures, but this technique is still inferior  
23 to the technique of the present invention as illustrated in Figure 2, for example.

24 It also should be noted that, unlike the technique depicted in Figure 1, wherein  
25 reverse polarity is applied, in the technique shown in Figure 2, voltage polarity is not

1 reversed. Polarity reversal is unnecessary because the parallel connection of the  
2 electrochemical cells effects bonding between all adjacent layers.

3 In Figure 2, each of the electrodes 203, 205, 207, and 209, as well as 202, 204, and  
4 206 is shown as contacting a minor surface of its respective layer. However, the  
5 invention is not so limited. The electrodes also may contact a limited portion of a major  
6 surface of a respective layer, while still achieving the salutary effects of the invention.  
7 Contact to major surfaces may be accomplished, for example, through the provision of  
8 suitable through holes in the appropriate layers, to ensure that proper electrode contact can  
9 be made with each layer.

10 Figures 3A and 3B show an alternate approach, which may be used in a  
11 circumstance in which it is difficult to contact all of the layers separately. As shown in  
12 Figure 3A, gaps 340 are formed in the silicon layer portions 308A, 310A, 312A, and  
13 314A. As illustrated in Figure 3B, with respect to the upper silicon layer 308, gaps 340  
14 are used to separate silicon layer 308 into silicon layer portions 308A and 308B.  
15 Electrical feedthroughs 320 are provided through glass layers 307, 309, and 311, as  
16 shown; these glass layers are continuous and do not include gaps. As illustrated by the  
17 combination of Figure 3A and Figure 3B, the provision of gaps 340 in portions of silicon  
18 layer 308 and in underlying silicon layers 310, 312, and 314, produces silicon layer  
19 portions 308A, 310A, 312A, and 314A, which creates a "block via" 330. By contacting  
20 an electrode 302 to the uppermost silicon layer portion 308A of the block via 330, it is  
21 possible to contact all of the glass layers 307, 309, and 311, achieving the same result as  
22 in the Figure 2 configuration. In this fashion, the block via 330 acts as an electrical  
23 feedthrough inside the stack 300. The block via 330 should be separated from the rest of  
24 the silicon-glass structure. This is because, when the DC voltage is applied, the electrode  
25 contacts shown in Figure 3 will cause sodium compounds (not shown) to form

1 throughout the interfaces between the silicon layer portions 308A, 310A, 312A, and 314A  
2 which are shown within block via 330 and the interfacing glass layers. However, because  
3 this block via 330 will have no function in the stack 300 other than to provide for  
4 electrode contact, weak bonding in this block via 330 will be irrelevant. All that is  
5 necessary to achieve this result is that the silicon layers in block via 330 make no  
6 electrical contact with any of the remaining portions of the silicon layers, 308B, 310B,  
7 312B, and 314B, which make up the device structure stack 350. Simultaneously, the block  
8 via 330 enables contact to all of the glass layers at once. As illustrated, all of the silicon  
9 layer portions are electrically connected by the electrical feedthroughs 320 to the bottom  
10 of the stack 300 which is setting on hotplate 306. In this fashion, parallel connection of  
11 the electrochemical cells, is accomplished when the DC voltage is applied.

12 Using the technique shown in Figure 3, formation of sodium compounds will  
13 occur on the layer interfaces of the block via 330 portion of stack 300, which is outside of  
14 the device stack 350. In the case where the device stack 350 is used in an electron optics  
15 microcolumn, this sodium compound formation will not have an adverse effect on the  
16 function of the microcolumn.

17 Figure 4A shows a schematic of a cross-section of a two layer prebonded stack  
18 400 of a silicon layer 412 and a glass layer 420. These layers were prebonded using a  
19 technique which permitted residual sodium compounds to be washed away. This  
20 prebonded stack 400 served as a starting point for the investigation of the migration of  
21 silicon during a bonding process. Figure 4B shows bonding stack 400 after the overlaying  
22 of an upper layer of silicon, 410, with subsequent anodic bonding using a conventional  
23 method for purposes of bonding upper silicon layer 410 to glass layer 420. A negative  
24 electrode contact 404 is applied to lower silicon layer 412 and a positive electrode contact  
25 402 is applied to upper silicon layer 410. Sodium compounds 460 have accumulated at

1 the interface 413 between the upper surface of lower silicon layer 412 and lower surface  
2 of overlying glass layer 420 during the bonding process. In addition sodium compounds  
3 460 have formed in adjacent regions, along the edge 422 of glass layer 420 and along  
4 exposed surface 424 of lower silicon layer 412, as illustrated in Figure 4C (which shows  
5 an enlarged area of Figure 4B). The accumulation of sodium compounds 460 along the  
6 edge 422 of glass layer 420 and along the exposed surface 424 of lower silicon layer 412  
7 is due to a sodium concentration gradient relative to adjacent surface 413.

8 Figure 5A shows a schematic of a cross-section of a two layer prebonded stack  
9 400 of a silicon layer 412 and a glass layer 420. These layers were prebonded using a  
10 technique which permitted residual sodium compounds to be washed away. Figure 5B  
11 shows bonding stack 400 after the overlaying of an upper layer of silicon, 410, with  
12 subsequent anodic bonding using one bonding technique of the present invention. In  
13 particular, a negative electrode contact 504 is applied to an upper surface 505 of glass  
14 layer 420, and a positive electrode contact 502 is applied to upper silicon layer 410.  
15 Sodium compounds 560 have accumulated only at the upper surface 505 of glass layer  
16 520 in the area of negative electrode contact 504. These sodium compounds 560 can  
17 easily be washed away. In this embodiment of the invention, the negative electrode  
18 contact 504 can be placed on a portion of the glass layer which avoids sodium compound  
19 formation in critical regions, as illustrated in the Figure 5C enlargement of a bonding area  
20 from Figure 5B.

21 Figure 6 shows a further embodiment of the invention. In this embodiment,  
22 silicon wafers 608, 610, 612, and 614 have been stacked in an offset manner relative to  
23 glass layers 607, 609, and 611. This leaves open spaces 618, 620, 622, and 624,  
24 respectively, on one side of the stack 600 and open spaces 617, 619, and 621 on the



1 opposite side of stack 600. Figure 6 shows a schematic of a cross-section of the silicon  
2 and glass wafers, so that only a portion of the offset pattern is shown..

3 Separate extended electrodes 640 and 650, which may be any desired conductive  
4 material, are then used in the manner shown, so that extended positive electrode 640  
5 contacts only silicon layers 608, 610, 612, and 614, while extended negative electrode 650  
6 contacts only glass layers 607, 609, and 611. In this fashion, it may be seen that the  
7 Figure 6 embodiment operates much like the embodiment shown in Figure 2, except that  
8 single extended electrodes 640 and 650 are used rather than a number of separate  
9 electrodes. As in the Figure 2 embodiment, by positioning the electrodes in this fashion,  
10 it is possible to avoid having sodium compounds form across an interface between the  
11 major surfaces of the adjacent layers. Rather, the sodium compounds 660 will form only  
12 where the extended electrode 650 is contacting the glass.

13 In the foregoing description, "glass" has been referred to generically and may be  
14 selected from any one of a number of different kinds of glass known in the art, or for that  
15 matter different kinds of glass which may be developed in the future. In addition, while  
16 silicon has been mentioned as the material involved in one of the anodically-bonded  
17 layers; this silicon may have only sufficient impurities or doping to permit adequate  
18 charge transfer or may be highly doped. Other conductive materials, including but not  
19 limited to other semiconductor materials, or metals, may be used, as previously mentioned  
20 herein. Clearly the number of layers to be anodically bonded may vary as desired.  
21 Moreover, while more silicon layers than glass layers are depicted in the foregoing  
22 examples, once again the invention is not so limited. Interleaving of layers of different  
23 materials *per se* is what is important.

24 While the invention has been described in detail above with reference to several  
25 embodiments, various modifications within the scope and spirit of the invention will be

- 1     apparent to those of working skill in this technological field. Accordingly, the scope of
- 2     the invention should be measured by the appended claims.